













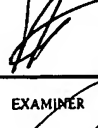
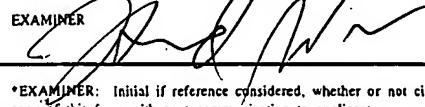
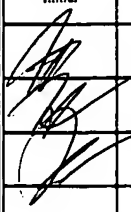


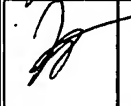
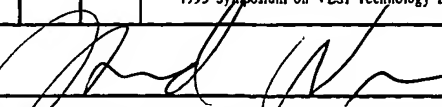



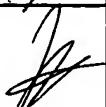

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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Luan Tran et al.				
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							Yes	No
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	AK								
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		Document Number	Date	Country	Class	Subclass	Translation		
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	AA						
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	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
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	AN						
	AO						
	AP						
	AQ						

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  	AR		V. Mathews et al., <i>Dry O₂ High Pressure Field Oxidation for 0.25 μm Isolation Technology</i> , SSDM '95 - Device and Process Technology, 2 pages.
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